Career Without Limits

TSMC will be in USA for recruitment…

If you are interested in reaching your career summit together with TSMC, send us your resume now!

Date & Location

10/17	San Diego, CA	10/27	Cambridge, MA
10/18	Los Angeles, CA	10/28	Stony Brook, NY
10/19	San Jose, CA	10/30	Pittsburgh, PA
10/20	Stanford, CA	10/31	Blacksburg, VA
10/21 – 22	Austin, TX	11/2	Ann Arbor, MI
10/23	Dallas, TX	11/3	Champaign, IL
10/25 – 26	Albany, NY	11/5	Gainesville, FL

Interview Application

(We keep your submissions confidentially)

Email your resume to campus@tsmc.com, marking "2014 US" before October 15th to sign up for private interview!

Video interview could be arranged for people who are unable to meet our delegates in person

Concise job information could be found in the following pages; visit our official website for details

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Job Openings

Function	#	Job Title	Job Description	Location
R&D	1	Advanced Lithography Engineer	1. Advanced lithography module process development and baseline sustaining. 2. Process stability/manufacturability improvement for yield and reliability qualification. 3. Process/tool transfer to volume manufacturing.	Taiwan (Hsinchu)
	2	Back End (BEOL) development Engineer	1. Advanced module process development and baseline sustaining. 2. Process stability/manufacturability improvement for yield and reliability qualification. 3. Process/tool transfer to volume manufacturing.	
	3	Computer Aided Design (TCAD) Modeling Engineer	1. Calibrate Transactions on Computer Aided Design (TCAD) environment through electrical and physical characterization of advanced technologies. 2. Work with device and integration teams to assist transistor technology development and strain modeling in advance technologies.	
	4	Extreme Ultraviolet Lithography (EUV) Mask Engineer	1. Technology development of Mask inspection. 2. Verify the Extreme ultraviolet lithography (EUV) mask inspection criteria. 3. Reach and develop E-beam inspection tool for mask defect detection. 4. Optical inspection tool verification.	
	5	Device Engineer/Manager	1. Device architecture definition. 2. Wafer Acceptance Test (WAT) analysis. 3. Transactions on Computer Aided Design (TCAD) co-work. 4. Simulation Program with Integrated Circuit Emphasis (SPICE) targeting.	
	6	Integration Engineer/Manager	1. Front End of Line (FEOL)/Mid End of Line (MEOL) Process integration. 2. Design rule and Logic cell layout/density evaluation. 3. Wafer Acceptance Test (WAT) data analysis and test pattern design. 4. Process reliability Qualification	

Function	#	Job Title	Job Description	Location
R&D	7	Litho/CMP/Wet Clean/Epi/Metal/Dielectrics Process Engineering/Manager	1. Enlarge process window and defect reduction. 2. Know hardware well and deliver CIPs for defect reduction. 3. Define roadmaps and drives improvements on device, quality, reliability, cost, yield, process stability, capability, and productivity for a new technology process.	Taiwan (Hsinchu)
	8	Resist Material Project Manager	1. Develop new generation litho resist material for advanced process application. 2. Hands-on experience on resist formulation tuning, litho relative material development to meet industry standard. 3. Knowledge in interface defect and cleaning control.	
	9	Optical proximity correction (OPC) Engineer	1. Recipe development for Optical proximity correction (OPC) recipes and multiple patterning decomposition recipes. 2. Optical proximity correction (OPC) taped-out layer sponsors. 3. Resolution enhancement technology development.	Taiwan (Hsinchu), North America
IC Design	10	CIS System & Application Engineer	1. Working with analog & digital designers to design and support CIS image capture system & evaluation cameras for CIS test chips and process development. 2. Develop and support CIS characterization methodology, timing control user interfaces, automatic data acquisition and analysis routines.	Taiwan (Hsinchu)
	11	Standard Cell Library Design Engineer	1. Standard Cell Circuit Design 2. Standard Cell Library Characterization 3. Standard Cell Library Silicon Validation 4. Standard Cell Test Architecture Development	
	12	Tech file/PDK Senior Engineer	1. Offer direct technical support to customers for techfile (DRC, LVS, RC extraction) or process design kit (PDK), either on-site or off-site 2. Provide timely response and high-quality solutions to resolve customers' techfile/pdk issues 3. Support techfile/pdk development especially for customers' customization requirements 4. Team work with TSMC HQ tech file & PDK teams	
	13	Standard Cell Library Design Technical Manager/Director	1. Standard Cell Circuit Design for low power or high speed chip implementation. 2. Standard Cell Library Silicon Validation. 3. Standard Cell Test Architecture Development.	

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IC Design	14	Design Flow & Methodology Development Architect/Technical Lead	1. Responsible for advanced Application-Specific Integrated Circuit (ASIC) design methodology definition, with the focus on signoff (Timing, IR/EM, power) and physical design, Place & Route (P&R) techniques for chip PPA boost of advanced nodes. 2. Lead technical direction of digital design solutions with tight collaboration with process R&D and Electronic Design Automation (EDA) partners. 3. Engage customers for technical consultation and discussion.	Taiwan (Hsinchu)
	15	Layout Engineer	1. Standard Cell, memory (SRAM,eDRAM,ROM, bit cell, pitch cell, IO & logic), Analog & Mixed signal layout. 2. Signals and Power buses planning. 3. Hook up from leaf cell to top level.	Taiwan (Hsinchu), North America
	16	(Senior) Physical Integration Engineer	1. Responsible for taping-out on high frequency embedded processors on the latest TSMC processes. 2. Duties will include synthesis, place-and-route, timing convergence, clock tree synthesis, noise, RV and ERC compliance and final database cleanup. 3. Will need to interface with partner teams for custom blocks and compiled memories and provide feedback to the library and process teams for power/performance/area optimizations.	Austin, TX
	17	Automatic Placement and Routing (APR) senior Engineer and technical Manager	1. Responsible for 16/10nm Electronic Design Automation (EDA)/router enablement, advanced chip implementation flow development, and chip PPA boost. 2. Act as the customer solution provider with headquarter.	
	18	Logic Design Technical Manager	Senior Logic Design Engineer responsible for architecting, implementing highly integrated and complex multifunctional SOC designs. 1. Generate or enhance SOC platforms that could incorporate processor, graphics, memory and high speed IO. 2. Manage and implement a complex Chip design from define the goals, requirements, execution plan, defining critical milestones, create the specification, Register-Transfer Level (RTL)coding to Physical Chip implementation. 3. System debugging from high level, logic level to circuit level. 4. Write detailed specifications; perform Static Timing Analysis (STA) timing, logic synthesis, lab debug and design verification. 5. Work closely with circuit, physical design, verification and software engineers to deliver logically correct and electrically robust designs.	San Jose, CA

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IC Design	19	(ASIC) Physical Design Technical Lead	Lead the Auto Place & Route Design Methodology technical development in San Jose on TSMC 16nm/10nm technologies 1. Work with process R&D teams at the headquarters to gain a deep understanding of technology capabilities and constraints. 2. Work with EDA vendors to enhance tool capabilities as well as with TSMC customers to understand design requirements of their SoC products. 3. Develop an effective APR design methodology & flow 4. Direct customer interface in training, debug and support role including development of App Notes and clear documentation. 5. Flexibility in expanding expertise to other technical areas over time like Static Timing Analysis (STA) or EM/IR. 6. Build a team over time and direct/mentor junior design engineers.	San Jose, CA
Manufacturing	20	Process/Process Integration Engineer	1. Maintain and control Inline defect baseline and excursion. 2. Responsibility for Technology yield/defect problem. 3. New technology defect study and early detection.	Taiwan (Hsinchu, Taichung, Tainan)
	21	Etch/Litho/CMP/Diffusion/Wet Clean/Epi Process Engineering Manager	1. Enlarge process window and defect reduction. 2. Know hardware well and deliver CIPs for defect reduction. 3. Define roadmaps and drives improvements on device, quality, reliability, cost, yield, process stability, capability, and productivity for a new technology process. 4. Improve process and equipment operational indicators - quality, cycle-time, capacity & cost. 5. Set up line defense system and meet tool and process matching requirements throughout start-up and ramp of new technology transfer.	Taiwan (Hsinchu, Taichung, Tainan)
	22	Process Integration Manager (Logic, Power IC, CIS, e-flash, MEMS)	1. Lead the team for the process integration and new product develop and ramp up. 2. New technology or customized technology transfer, installation, qualification, volume production ramping and sustaining smooth production. 3. Responsible for WAT trouble shooting, yield improvement & cost reduction driving.	Taiwan (Hsinchu, Taichung, Tainan)
	23	Big Data Manager	1. Lead the team on the use of chosen technologies to design Big Data analysis solutions for semiconductor manufacturing, per current and emerging industry trends and standards. 2. Communicate directly with internal partners and users; gathering requirements, ensuring appropriate solutions. 3. Manage multiple projects including analysis methodology design, solution development and technical infrastructure.	Taiwan (Hsinchu)
	24	N16/N10 FinFET Device Technical Manager	1.FinFET device design and yield ramp-up. 2.Involve and work with RD in early stage to develop N16 FinFET device.	

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Manufacturing	25	Product Engineer (Power Technology)	1. Assist new developed power technology stepping into production through solving issues in R&D phase, Failure Analysis skill, product circuit analysis, strengthen design flow. 2. Power device characterization, device design and performance analysis. 3. Co-work with RD/Module/QR/PDK teams to deliver new technology. 4. Enhance existing design flow/kits, build competitive/cost-effective/customized environment for pioneer customer.	Taiwan (Hsinchu)
	26	Quality & Reliability Engineer (Q&R)	Advanced Device Technology 1. Device reliability (BTI/HCI) test execution for process development and qualification. 2. Reliability Model/Physics study for new advanced technology development. Package Qualify 1. Quality & reliability gating for far back-end new development technology transfer to production. 2. Identify CPI (Chip-Packaging-Integration) reliability risk and performance, ensure IC packaging/substrate quality for advanced far back-end technology. 3. Co-work with engineering team and customer to resolve IC packaging/substrate assembly technology reliability issues. Material Quality 1. Incoming raw material quality & reliability enhancement. 2. Raw material supplier quality management including new supplier/material evaluation, supplier process change management, complaint case handling, etc.	
	27	System Reliability Manager/Director (Q&R)	1. Lead reliability department that responsible for the system level reliability development and validation from product development to the high volume manufacturing. 2. Collaborate with both internal and customer design teams to drive the hardware and software design development, test, and resolutions. 3. Work with R&D to solve module, device, and product reliability issues for advanced technology development and high volume manufacturing.	Taiwan (Hsinchu)
	28	Advanced Hardware Improvement Program Director	1. Early involve in new generation logic technology development. 2. Hands-on experience on hardware improvement. 3. Program schedule control and resource arrangement.	Taiwan (Tainan)

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Business	29	IT Engineer	1. Project management and System development/maintenance to realize customers IT requests. 2. System development/maintenance to sustain user operation and support for enabling internal project. 3. Role play as the system consultant for supporting site operation support team to smooth business operation.	Taiwan (Hsinchu, Taichung, Tainan)
	30	Corporate Planning Engineer	1.Capacity planning and management. 2.Productivity improvement. 3.Capital investment evaluation and control. 4.Fab. layout planning.	Taiwan (Hsinchu)
	31	Accounting Associate	1. Rotate within Accounting: Accounting Operations, Accounting Services and Financial Forecasting, Planning, Reporting & Analysis Department. 2. Preparation of financial Static Timing Analysis statements, including analyze, summarize, record and report data.	
	32	Corporate Finance Associate	1.Rotate among 2~3 functions within a timeframe of 3 years+. Such functions include treasury operations, Financial Planning, Customer Credit, Insurance, Financial Risk Management, SEC Compliance and Investment Management. 2.Job scope includes funding, forex risk management, debt/equity offerings, investment valuation, various projects to support management decisions, credit risk management, multiple insurance programs to reduce TSMC's operating risk, financial risk control/modeling, R.O.C./U.S. Securities and Exchange Commission (SEC) compliance, and post-investment management.	
	33	Business Lawyer	1. Drafting and negotiating contracts (joint development agreements, business agreements, technology transfer/license agreements and other commercial agreements). 2. Advising internal clients on transactional and regulatory issues. 3. Drafting and enforcing company policy on protection of technology. 4. Supporting litigation.	
	34	Patent Attorney	1. Drafting and prosecuting patent applications before the United States Static Timing Analysis Patent and Trademark Office (USPTO) and other foreign jurisdictions. 2. Review draft patent applications and office actions prepared by outside counsel for domestic and foreign filings. 3. IP licensing related activities and litigation support. May have the opportunity to handle a variety of other IP issues including patents and trade secret matters, claim construction, opinions on patent infringement and validity.	
	35	HR Specialist	In TSMC HR team environment, you will get opportunities to work with the most dynamic HR professionals in staffing, Recruiting, Compensation & Benefits, Training & Development, Employee Relation, etc. Our rotation program will help you discover your passion in a particular HR interest or expend your knowledge in every function within HR.	